30V N-Ch Power MOSFET

Feature

DS

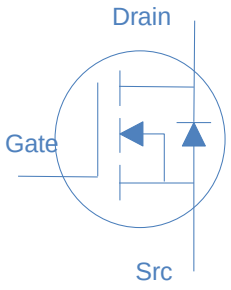
DS(on),typ GS Ω

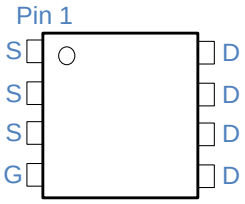
- High Speed Power Switching, Logic Level
- Enhanced Avalanche Ruggedness
- 100% UIS Tested, 100% Rg Tested
- Lead Free, Halogen Free

Application

- Hard Switching and High Speed Circuit
- DC/DC in Telecoms and Inductrial

DFN3*3





=25 (unless otherwise specified)

Parameter	Symbol	Conditions
Continuous Drain Current (Silicon Limited)		
Drain to Source Voltage	DS	
Gate to Source Voltage	GS	
Pulsed Drain Current		
Avalanche Energy, Single Pulse	AS	

Symbol

Thermal Resistance Junction-Case

Electrical Characteristics at T =25 (unless otherwise specified)

Static Characteristics

Parameter	Symbol	Conditions				
				typ		
Drain to Source Breakdown Voltage	(BR)DSS	GS=0V, I μ				
Gate Threshold Voltage	GS(th)	GS DS, I μ				
Zero Gate Voltage Drain Current	DSS	GS=0V, V_{DS}=24V, T =25				μ
		GS=0V, V_{DS}=20V, T =125				
Gate to Source Leakage Current	GSS	GS=±20V, V_{DS}				
Drain to Source on Resistance	DS(on)	GS=10V, I				Ω
		GS=4.5V, I				
Transconductance	fs	DS=5V, I				S
Gate Resistance		GS=15mV, V_{DS} =0V, f=1MHz				Ω

Dynamic Characteristics

Input Capacitance		GS=0V, V_{DS}=15V, f=1MHz		2979		pF
Output Capacitance						
Reverse Transfer Capacitance	rss					
Total Gate Charge	(10V)	=15V, I =30A, V_{GS}				
	(4.5V)					
Gate to Source Charge						
Gate to Drain (Miller) Charge	gd					
Turn on Delay Time	d(on)	=15V, I =1A, V_{GS}=10V, =2.7Ω,				
	r					
Turn off Delay Time	d(off)					
Fall Time	f					

Reverse Diode Characteristics

Diode Forward Voltage	SD	GS=0V, I_F=37A				
Reverse Recovery Time	rr	F=37A, dI_F/dt=100A/μ				
Reverse Recovery Charge	rr					

Fig 1. Typical Output Characteristics	Figure 2. On-Resistance vs. Gate-Source Voltage

Figure 3. On-Resistance vs. Drain Current and Gate Voltage	Figure 4. Normalized On-Resistance vs. Junction Temperature

Figure 5. Typical Transfer Characteristics	Figure 6. Typical Source-Drain Diode Forward Voltage

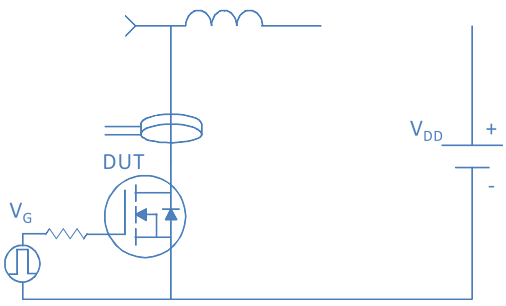
Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage	Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

Figure 9. Maximum Safe Operating Area	Figure 10. Single Pulse Maximum Power Dissipation

Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient

Inductive switching Test	

Gate Charge Test	

Uclamped Inductive Switching (UIS) Test	
	

Diode Recovery Test	

Package Outline

DFN3*3_P, 8leads

Dimension in mm